IN THE SPECIFICATION

Please amend the specification as follows:

Please amend page 8, Paragraph 0035 which begins on line 8, as follows:

In Figs. 4A and 4B, an amorphous silicon layer (a-Si layer, not shown) is deposited on the gate insulation layer 330, and then a doped amorphous silicon layer (e.g. n^+ α-Si, not shown) is deposited on the amorphous silicon layer. Next, a second photolithography (PEP II) is performed, and part of the doped amorphous silicon layer and the amorphous silicon layer are etched to form a semiconducting island on the gate insulation layer 330 in the transistor area 302. ~~Thesemiconducting~~ The semiconducting island is composed of a patterned amorphous silicon layer 410 and a patterned doped amorphous silicon layer 420.

Please amend page 8, Paragraph 0036 which begins on line 15, as follows:

In Figs. 5A and 5B, a conductive layer (not shown) is deposited on the gate insulation layer 330 and the semiconducting island. The, a third photolithography (PEP III) is performed to remove part of the conductive layer (not shown), and a longitudinally extending common line 510 and a longitudinally extending data line 520 are formed on the gate insulation layer 330, and simultaneously, a source electrode 530 and a drain electrode ~~546~~ 540 are formed on the doped amorphous silicon layer 420. Then, using the source electrode 530 and the drain electrode 540 as a mask, part of the doped amorphous silicon layer 420 is etched to expose part of the surface of the amorphous silicon layer 410. Thus, a thin film transistor (TFT) structure is obtained in the transistor area 302. Also, the drain electrode 540 electrically connects the data line 520.

Please amend page 10, Paragraph 0044, which begins on line 17, as follows:

Next, a longitudinally extending common line 510 and a longitudinally extending data line 520 are formed on the gate insulation layer 330, and simultaneously, a source electrode 530 and a drain electrode 540 are formed on the doped amorphous silicon layer 420. Then, using the source electrode 530 and the drain electrode 540 as a mask, part of the doped amorphous silicon layer 420 is etched ~~Ito~~ to expose part of the surface of the amorphous silicon layer 410. Thus, a thin film transistor (TFT) lying on the gate line 310 is obtained. Also, the drain electrode 540 electrically connects the data line 520. Next, a first conductive layer 610 is formed on the gate insulation layer 330 in the capacitor area 301 and covers the common line 510. The first conductive layer 610 serves as a bottom electrode or a pixel electrode.

Please amend page 11, Paragraph 0045, which begins on line 3, as follows:

Next, a conformal passivation layer 710 is formed on the gate insulation layer 330, the first conductive layer 610, the TFT structure, the data line X520 and the gate line 310. Then, by photolithography, a first via hole 720 penetrating the passivation layer 710 is formed to expose the surface of the source electrode 530. ~~The dielectric layer of a capacitor.~~

Please amend page 11, Paragraph 0046, which begins on line 7, as follows:

Next, a planarization layer 810 is formed on the passivation layer 710 and fills the first via hole 720. Then, by photolithography, a second via hole 820' and a third via hole ~~passivation layer 710 serves as a 830 penetrating the planarization layer 810~~ 830 are formed. The second via hole 820' exposes the surface of the source electrode 530 and the surface of the passivation layer 710 in the transistor area 302. The third via hole 830 exposes the

surface of the passivation layer 710 by penetrating the planarization layer 810 in the capacitor area 301.